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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/204,479	12/03/98	TREMBLAY M	SP-3289US

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ENG, D	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary

Application No.	Applicant(s)
09/204,479	Tremblay et al.
Examiner	**Art Unit**
David Y. Eng	2155

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 4, 2001*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 3-17, and 19-22* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3-17, and 19-22* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

Claims 2 and 18 have been cancelled. The active claims are 1, 3-17 and 19-22.

Claims 1, 3-17 and 19-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Scope of claim 1 is not clear. The claim fails to recite functional relationship between the register file, the decoder and the functional unit. It is not clear how the register file and the functinal unit are related to deriving register spedifier by the decoder. The functional unit and the register file as recited are neither helping the decoder to derive specifier nor using the derived specifier.

In claim 4, there is no functional relationship between the components of claim 4 and parent claim 1. The term "said" should be used if claim 4 further limits the components of parent claim 1. Other claims have similar defect. See the decoder in claim 17 for example.

In claim 7, it is not clear how the recitation in lines 5-8 is related to control transfer.

With respect to claim 19, it is not clear what is meant by "the register file generating two pointers". Note that a register file is for storing or outputting operands in response to register specifiers. A register file does not generate pointers.

Further with respect to claims 1, 3-16, there is nothing recited in the claims to execute instructions in a manner as recited in dependent claims 3-16.

Scope of limitation of the following is not clear:

1. "the instruction in which a register specifier is implicitly derived" in line 5 of claim 1. Note that an instruction by itself can not derive anything. An instruction is nothing more than a command.

2. "the processor is a Very Long Instruction Word" in claim 4. A processor is not a word.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 3-17 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanenbaum (text book) in view of Fleck.

Figure 3-17 of Tanenbaum shows numerous format that an instruction can have. Figure 3-16 shows an instruction having having 4 fields, namely, an opcode field and 3 address or operand fields. Each of the addres fields contains an address of an operand stored in a register or in a memory location. The opcode field contains an operation of any types to be performed on two of the operands and the result is stored in the third operand address. From Figure 3-16, it is clear that an instruction having fields containing operand addresses and opcodes is well known in the art. It is further well known that opcodes can be of any type, for examples, combination of multiplication, division, substraction or addition on operands represented by integer, floating point of single or double precision (see section 3.3 ADDRESSING, page 79-80).

The operand addresses shown in Figure 3-16 are explicit address. The drawing does not show deriving implicit address from explicit address. The technique is called "indexing" or "autoindexing" which is taught in section 3.3.5 INDEXING (page 84-85) of Tanenbaum. The section also discloses that indexing is used in IBM 370 and PDP11.

Tanenbaum fails to show that IBM 370 or PDP11 or any computer having basic components such as register file, decoder and functional unit. However, Fleck taught that, as admited by applicants, register file, decoder and functional units are basic components of a computer. From the teaching of Tanenbaum and Fleck, it would have been obvious to a person of ordinary skill in the art to implement indexing on a computer having register file, decoder and functional unit having any types of instruction sets.

Claims 1, 3-17 and 19-22 are provisionally rejected under the judically created doctrine of obviousiness-type double patening as being unpatentable over claims 1-29 of copending Application No. 09/204,585 in view of Tanenbaum. The claims of 09/204,585 recites a plurality of functional units, a decoder and a register. The claims do not state how addresses of register file are formulated. However, Figure 3-16 of Tanenbaum teaches how register addresses are implicitly derived from explicit addresses. Since both references are directed toward addressing register file, it would have been obvious to a person of ordinary skill in the art to formulate register addresses as taught by Tanenbaum so that address field in an instruction can be shorter.

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

DAVID Y. ENG
PRIMARY EXAMINER